CLAIMS

WHAT IS CLAIMED IS:

1. A system, comprising:

a processor;

a bridge coupled to the processor;

a memory selectably coupled to the bridge and the processor; and

a switching mechanism coupled between the memory and each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory.

2. The system of claim 1, further comprising:

control logic coupled to the switching mechanism for controlling changes between the first state and the second state.

3. The system of claim 2, further comprising:

a second bridge coupled between the bridge and the processor, wherein the control logic is comprised within or controlled by the second bridge.

4. The system of claim 2, wherein the control logic is comprised within or controlled by the processor.

5. The system of claim 2, further comprising:

a crypto-processor coupled to the memory, wherein accesses to the memory pass through the crypto-processor.

6. The system of claim 5, wherein the control logic is comprised within or controlled by the crypto-processor.

7. The system of claim 1, further comprising:

a crypto-processor coupled to the memory, wherein accesses to the memory pass through the crypto-processor.

8. The system of claim 7, wherein the crypto-processor is further coupled to the switching mechanism; and wherein the switching mechanism couples the crypto-processor to the processor in the first state and to the bridge in the second state.

9. The system of claim 5, further comprising:

a local bus;

a first I/O bus;

a second I/O bus; and

a second bridge coupled between the bridge and the processor, wherein the second bridge is coupled to the processor through the local bus, and wherein the second bridge is coupled to the bridge through the first I/O bus; and

wherein the crypto-processor is coupled to the processor through the local bus in the first state, and wherein the crypto-processor is coupled to the bridge through the second I/O bus in the second state.

10. The system of claim 1, wherein the memory and the bridge are coupled to an I/O bus; wherein the bridge further comprises I/O bus interface logic for communicating on the I/O bus; wherein the processor further comprises I/O bus interface logic for communicating on

the I/O bus; wherein the switching mechanism is coupled to the I/O bus; wherein the processor is coupled to the switching mechanism through the I/O bus interface logic; wherein the first state comprises the I/O bus interface logic of the processor being configured to communicate with the memory over the I/O bus, and wherein the second state comprises the I/O bus interface logic of the bridge being configured to communicate with the memory over the I/O bus.

11. The system of claim 1, wherein the second I/O bus comprises an LPC bus.

12. The system of claim 1, wherein the memory is a ROM or flash memory.

13. The system of claim 12, wherein the ROM or the flash memory includes a BIOS ROM.

14. A method for operating a computer system comprising a processor, a memory, and a first device, wherein the processor is operably coupled to the first device, and the first device is operably coupled to the memory, the method comprising:

coupling the processor and the memory using a switching mechanism, wherein the switching mechanism is configured to operate in a first state operably coupling the first device to the memory and a second state operably coupling the processor to the memory;

switching the computer system into the second state, thereby operably coupling the memory to the processor using the switching mechanism; and

reading from the memory in the second state.

15. The method of claim 14, wherein the processor is coupled to the first device through at least a system bus, wherein the first device is coupled to the memory through a first I/O bus, wherein coupling the processor and the memory using the switching mechanism comprises coupling the processor to the first I/O bus through the switching mechanism.

16. The method of claim 14, wherein the second state comprises booting the computer system, wherein the memory comprises a ROM, and wherein reading from the memory comprises reading BIOS information from the ROM.

17. The method of claim 14, wherein the memory comprises secure storage, wherein the second state comprises reading from the secure storage, and wherein reading from the memory comprises reading secure data from the secure storage.

18. The method of claim 14, further comprising:

switching the computer system into the first state.

19. The method of claim 18, further comprising:

reading from the memory in the first state.

20. A computer system comprising:

a processor;

a memory;

a first device operably coupled to the processor and to the memory;

means for switching between a first state where the first device is operably coupled to the memory and a second state where the processor is operably coupled to the memory; and

means for controlling the means for switching.

21. The computer system of claim 20, further comprising:

a crypto-processor coupled to the memory, wherein accesses to the memory pass through the crypto-processor.

22. The system of claim 21, wherein the crypto-processor is further coupled to the switching mechanism; and wherein the switching mechanism couples the crypto-processor to the processor in the first state and to the bridge in the second state.

23. A computer system, comprising:

means for switching the computer system from a first state to a second state, thereby operably coupling a memory to a processor in the second state;

means for coupling the processor and the memory using the means for switching, wherein the means for switching is configured to place the computer system in a first state operably coupling the a device to the memory and in a second state operably coupling the processor to the memory;

means for reading from the memory in the second state; and

means for reading from the memory in the first state.

24. A computer readable program storage device encoded with instructions that, when executed by a computer system comprising a processor, a memory, and a first device, wherein the processor is operably coupled to the first device, and the first device is operably coupled to the memory, performs a method of operating the computer system, the method comprising:

coupling the processor and the memory using a switching mechanism, wherein the switching mechanism is configured to operate in a first state operably coupling the first device to the memory and a second state operably coupling the processor to the memory;

switching the computer system into the second state, thereby operably coupling the memory to the processor using the switching mechanism; and

reading from the memory in the second state.

25. The computer readable program storage device of claim 24, wherein the processor is coupled to the first device through at least a system bus, wherein the first device is coupled to the memory through a first I/O bus, wherein coupling the processor and the memory using the switching mechanism comprises coupling the processor to the first I/O bus through the switching mechanism.

26. The computer readable program storage device of claim 24, wherein the second state comprises booting the computer system, wherein the memory comprises a ROM, and wherein reading from the memory comprises reading BIOS information from the ROM.

27. The computer readable program storage device of claim 24, wherein the memory comprises secure storage, wherein the second state comprises reading from the secure

storage, and wherein reading from the memory comprises reading secure data from the secure storage.

28. The computer readable program storage device of claim 24, the method further comprising:

switching the computer system into the first state.

29. The computer readable program storage device of claim 28, the method further comprising:

reading from the memory in the first state.